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POWER MOSFET DEVICE WITH REDUCED  
SNAP-BACK AND BEING CAPABLE OF  
INCREASING AVALANCHE-BREAKDOWN  
CURRENT ENDURANCE, AND METHOD  
OF MANUFACTURING THE SAME

Abstract of the Invention

The invention disclosed a power MOSFET with reduced snap-back and being capable increasing avalanche-breakdown current endurance, which has sequentially a drain with  $N^+$  silicon substrate, an  $N^-$  epitaxial layer formed on said  $N^+$  silicon substrate, a source contact region formed of  $N^+$  doped well and  $P^+$  doped well implanted after etching in a  $P^-$  well formed on said  $N^-$  epitaxial layer, and a gate electrode with deposition of polysilicon above a channel between said  $N^-$  epitaxial layer and  $N^+$  source contact region, said device is characterized in that: Said source contact region is formed by etching into said  $P^-$  well first and implanting  $P^+$  dopant to the interface between said  $N^-$  epitaxial layer and  $P^-$  well, and the source contact region of said  $N^+$  well and that of said  $P^+$  well are not at the same level, by which it is possible to increase the avalanche-breakdown current endurance of the power MOSFET device.